CHANDIGARH ENGINEERING COLLEGE- CGC, LANDRAN, MOHALI

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

Assignment 2

Subject and Subject code: Digital System Design BTEC– 302 -18
Semester: 3rd
Date on which assignment given: 11-11-2022
Date of submission of assignment: 18-11-2022

Note: Each question carries 2 marks **Total marks:10**

Course Outcomes

CO 1	Apply concepts of Boolean algebra for handling logical expressions.
CO 2	Understand working and realization of combinational logical expressions.
CO 3	Understand working flip-flops and use them in designing of sequential circuits.
CO 4	Understand fundamental concepts of logic families and architectural of programmable devices.
CO 5	Use HDL programming tool for simulation of combinational and sequential circuits

Bloom's Taxonomy Levels

L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing, L5 – Evaluating, L6 - Creating

Assignment related to COs	Relevance to CO No.	Bloom's Level
Q1. Design a Decade Asynchronous counter.	CO-3	L6
Q2. Convert J-K Flip-Flop to T-type flip flop.	CO-3	L2
Q3 What are Shift Registers? Draw and explain Universal shift register.	CO-3	L1
Q4. Why do we need A/D converters? Explain the working of Dual slope A/D converter using suitable block diagram.	CO-4	L4
Q5. a) Design a 3-bit Binary to Gray Code Converter using Programmable Logic Array. b) Explain the following characteristics of Digital Logic Families: 1. Propagation Delay 2. Noise Margin	CO-4	L6, L4